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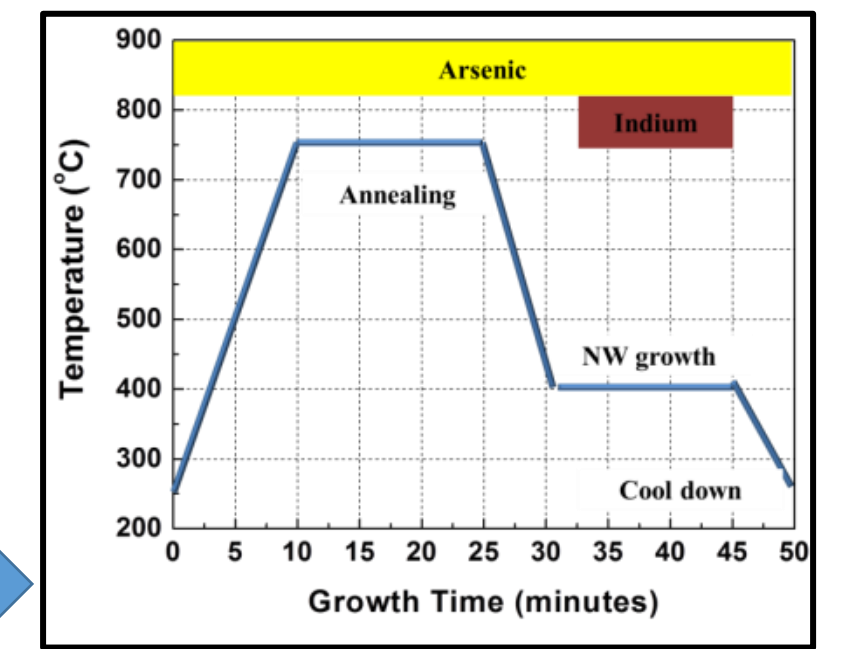
Motivation

- Au-free growth of NWs is fundamental for:
 - optical applications, to avoid the effect of Au impurities in the semiconductor
 - Si CMOS integration, incompatible with Au
- InAs NWs:
 - high electron mobility
 - low bandgap and possible band engineering with compatible barrier materials (InP, GaAs, GaSb)
 - easy fabrication of high performance leads

Growth technique (CBE)

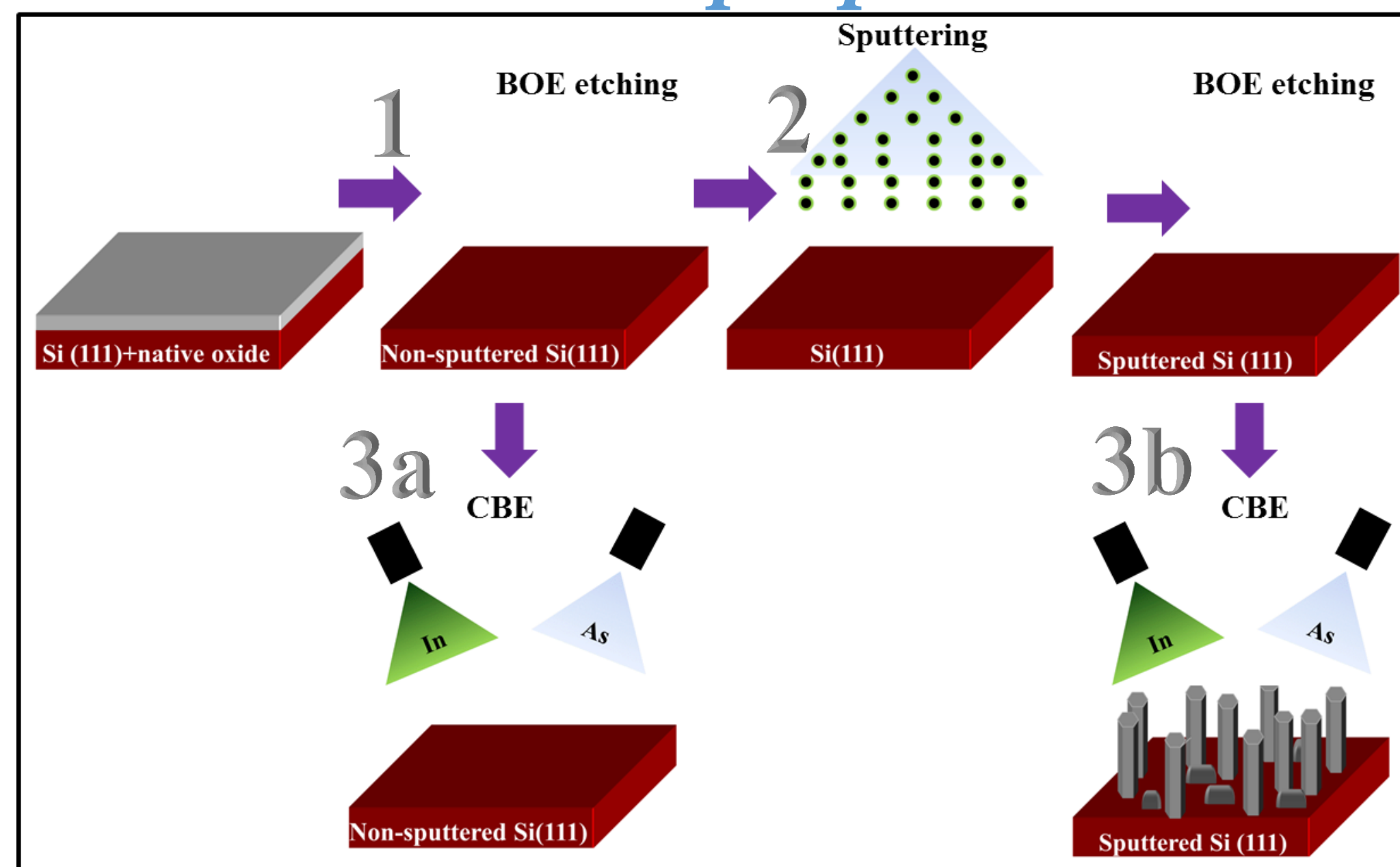


- UHV epitaxial growth (base pressure = 10^{-10} Torr)
- Load lock and intermediate buffer chamber to avoid contaminants
- Heated sample holder (up to $\sim 800^\circ\text{C}$)
- Gas-phase metalorganic precursor (TBAs, TMIn) flow regulated through line pressure ($P_{\text{TBA}s}$ and P_{TMIn}) control
- TBAs pre-cracked in high temperature (1000°C) injector
- Two stage growth protocol: HT annealing step under As flux and NW growth



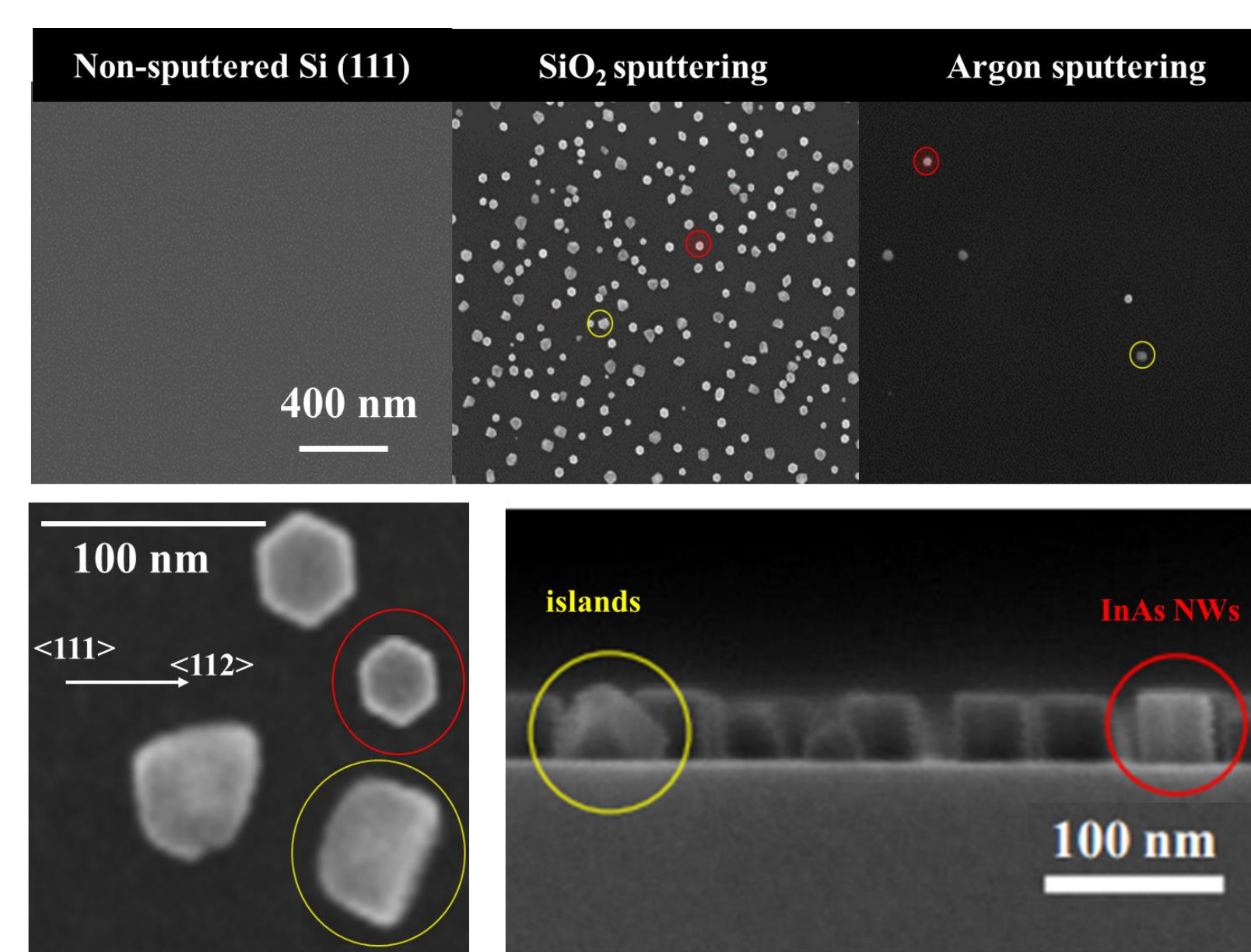
Si substrate preparation and InAs NW growth

Si substrate preparation



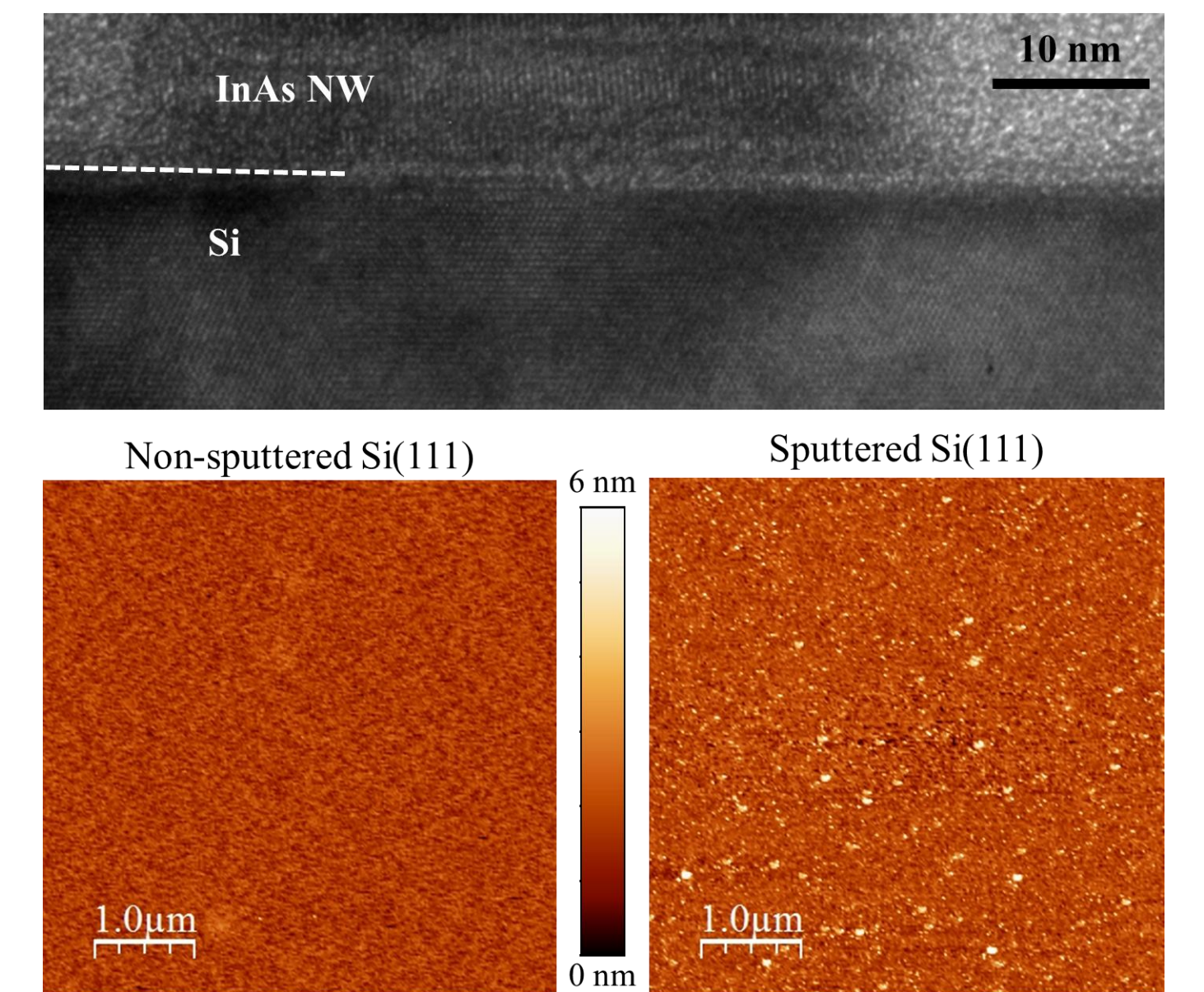
- Step 1** → Commercial Si 111 wafers buffered HF etch (2') for native oxide removal
- Step 2** → Sputter coat with few (1-20) nm SiO₂ + Buffered HF etch (2') for sputtered oxide removal or Ar⁺ sputter with DC gun or with AC plasma
- Step 3** → InAs NWs growth by CBE on: a) non sputtered and b) sputtered Si (111) substrates

SEM characterization



- Controlled sputtering of the Si(111) surface enhances the nucleation of InAs crystals (NWs and islands), while no nucleation occurs on non-sputtered Si(111) surfaces under identical growth conditions.
- The yield (Y) of NWs, determined as NW density/total crystal (NWs + islands density) is ~ 0.5 for both SiO₂ and Ar sputtered samples

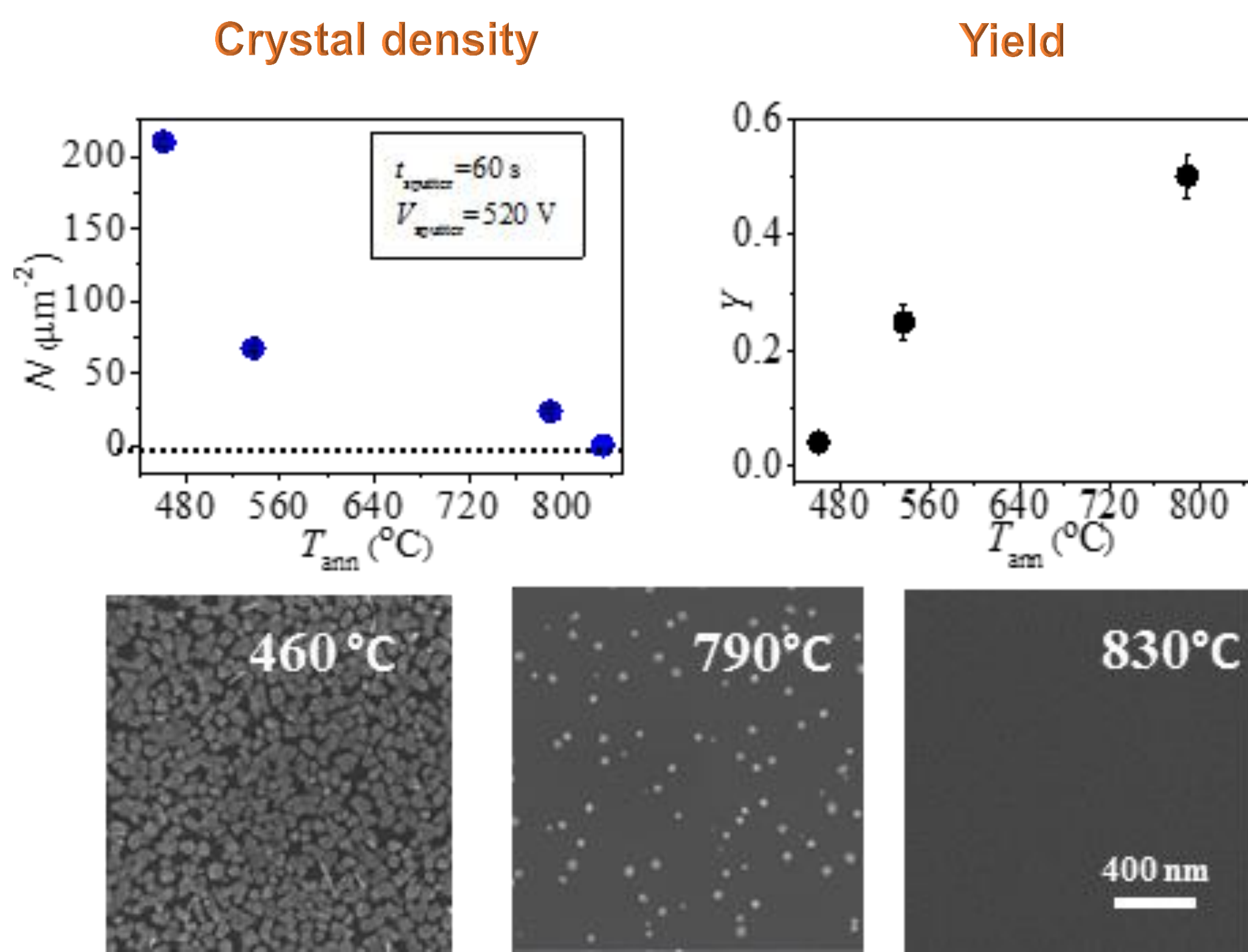
Nature of nucleation sites



- HRTEM analysis shows defect-free crystalline order of the sputtered Silicon substrates after growth.
- AFM scans show comparable surface roughness.
- Amorphization and roughness are unlikely to be the source of nucleation sites, which may be instead surface defects associated with the sputtering process that serve as preferential physical nucleation sites.

Impact of growth parameters

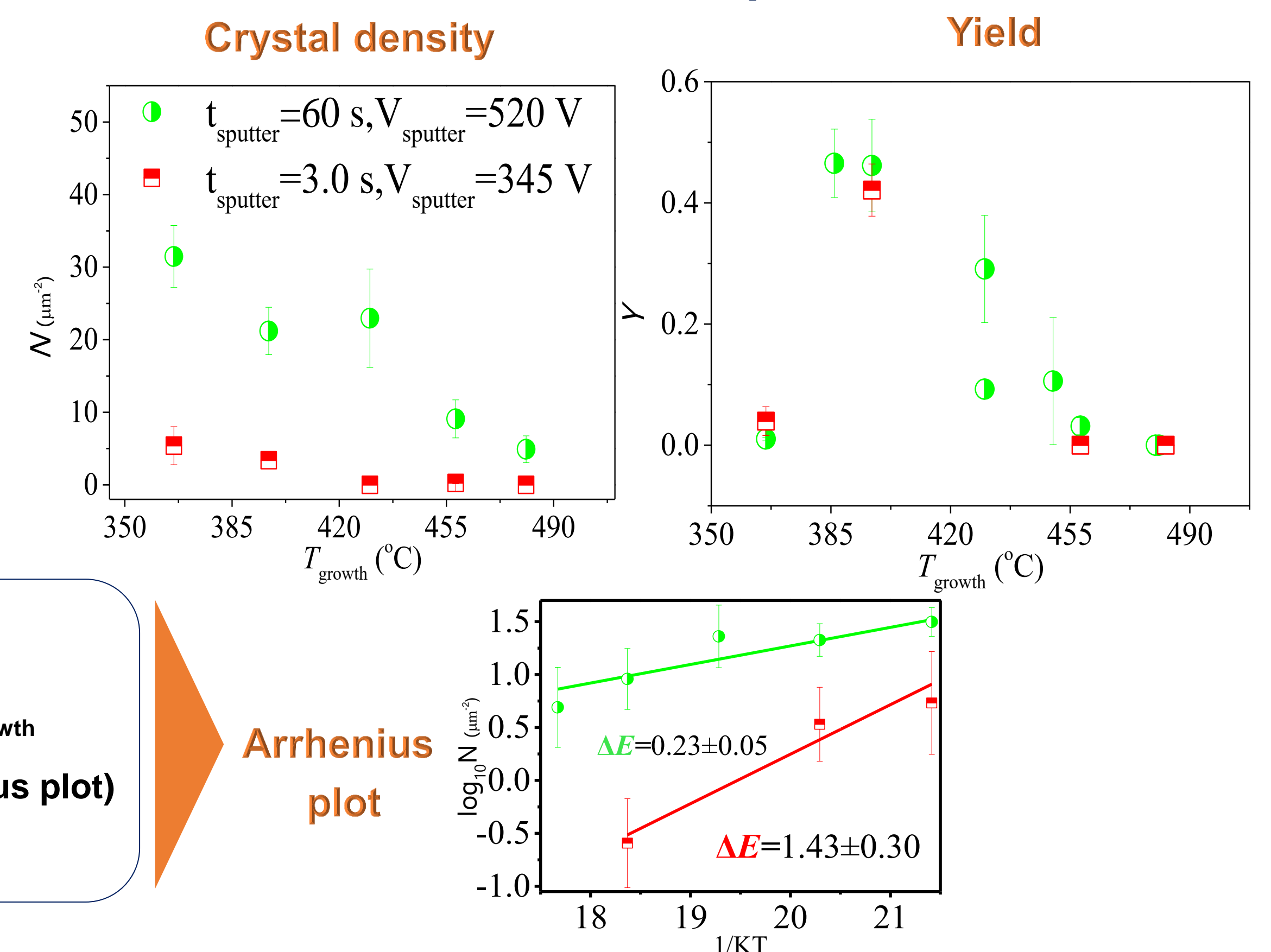
Annealing temperature



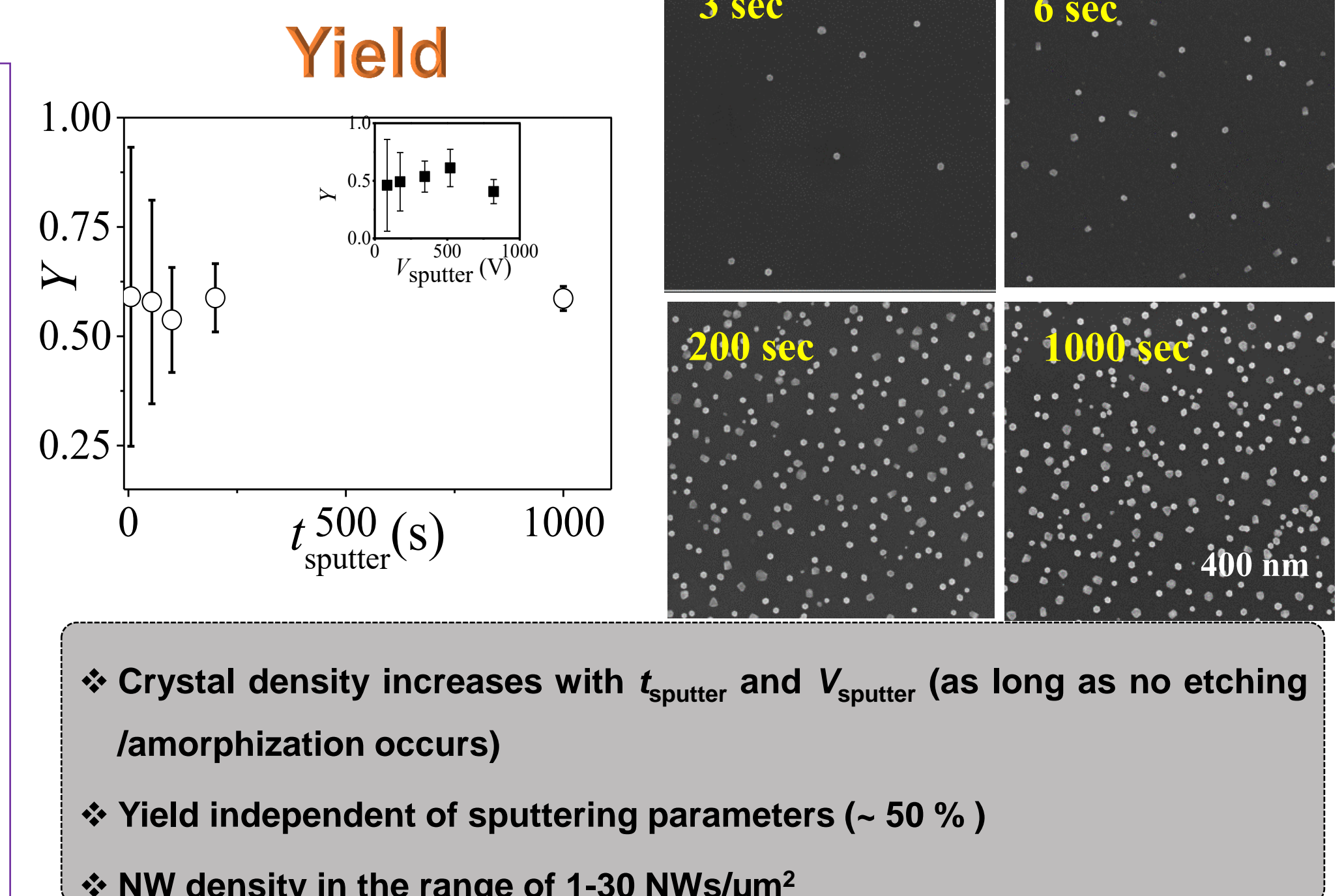
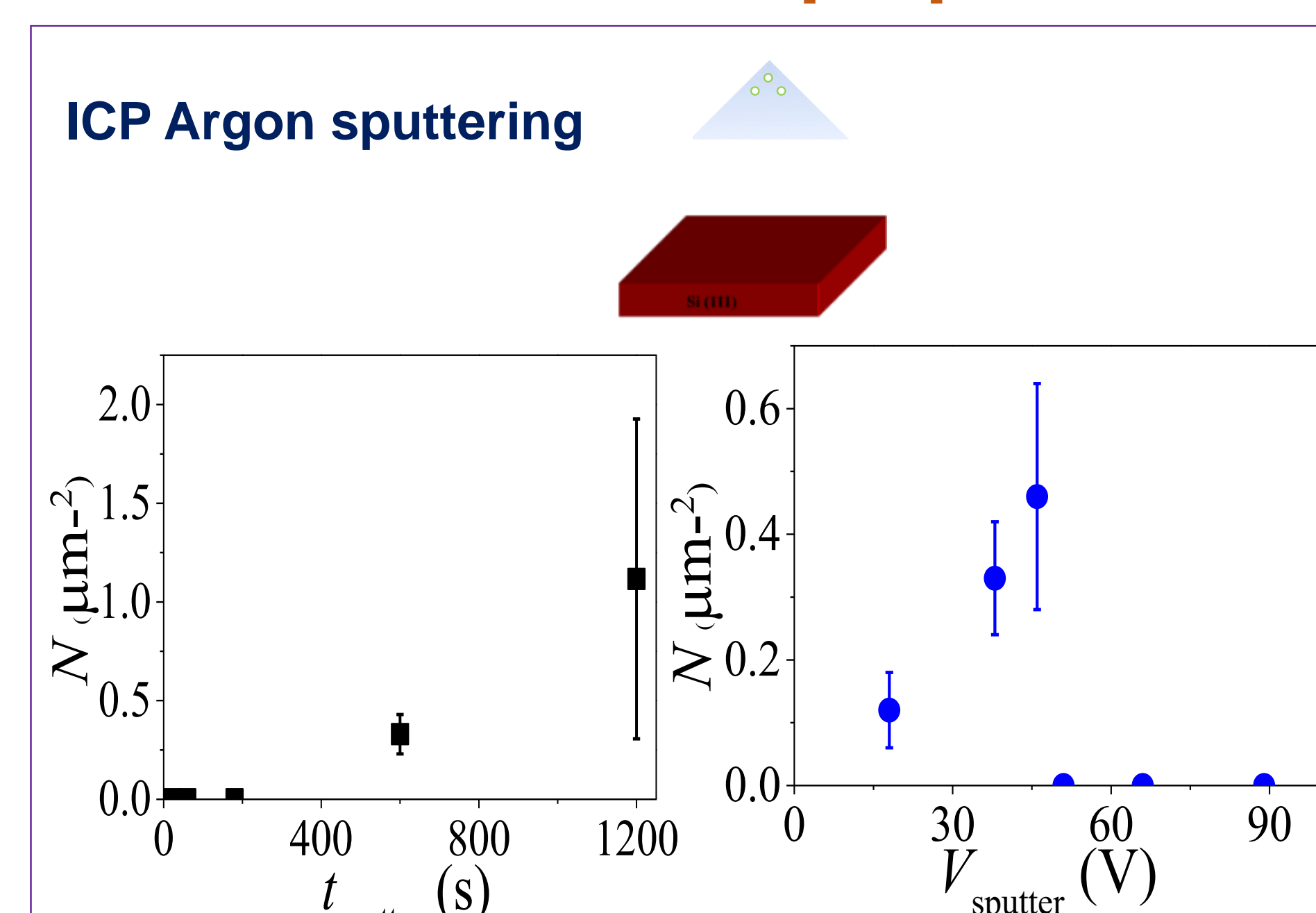
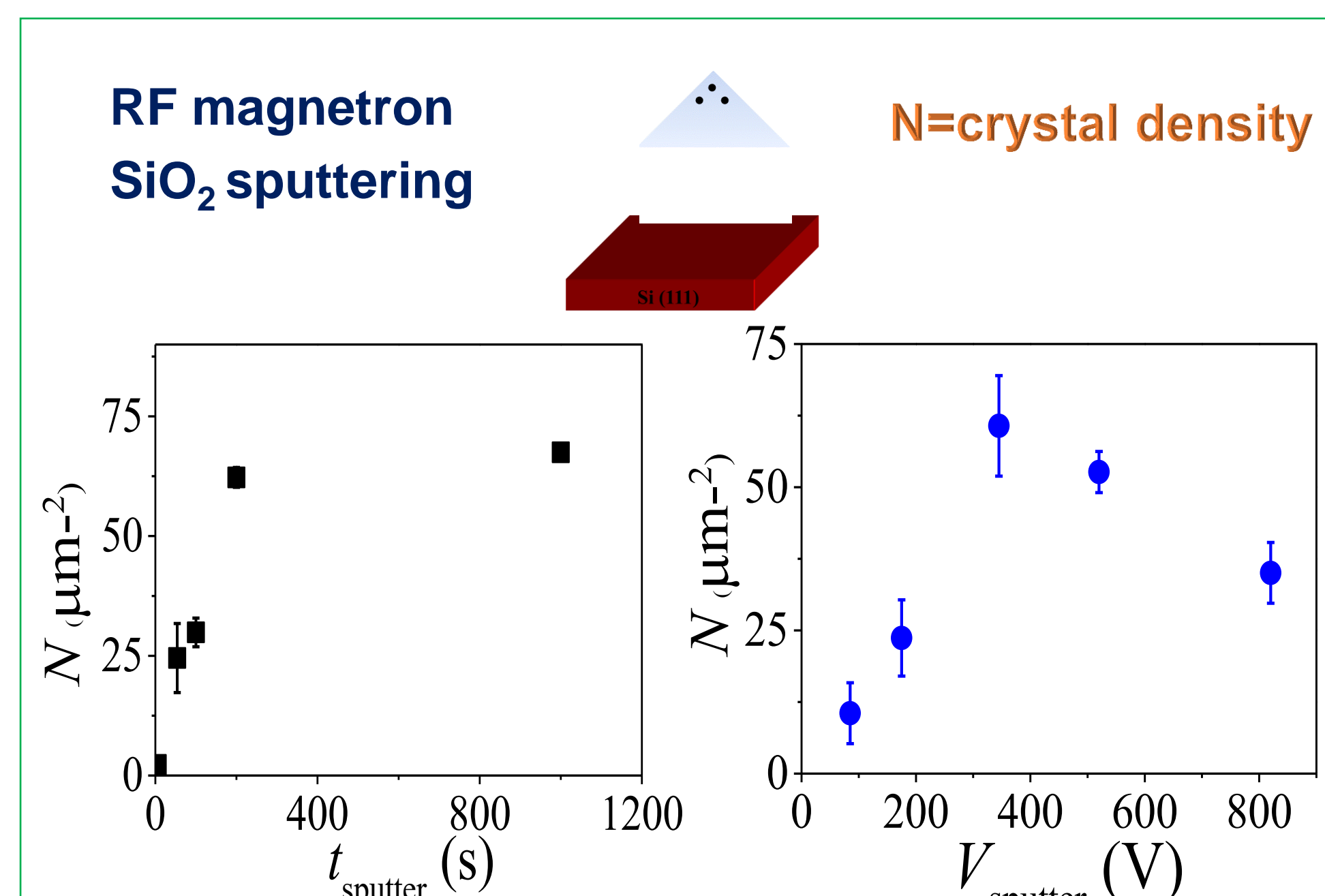
- Annealing reorders the Si (111) surface
- Defect density decreases and crystal density decreases
- Yield increases with annealing temperature
- Highest yield of NWs at 790°C

- $T_{\text{ann}} = 790^\circ\text{C}$, $t_{\text{growth}} = 15$ mins
- InAs crystal density decreases with T_{growth}
 - High V_{sputter} and t_{sputter} : low ΔE (Arrhenius plot)
 - NW yield maximum (~ 0.5) at 400°C

Growth temperature



Role of substrate preparation



Conclusions

- InAs crystals nucleate on sputtered Si(111) surfaces while no nucleation occurs on nonsputtered Si(111) surfaces.
- The InAs crystals nucleating on the sputtered silicon surfaces consist of InAs NWs and parasitic islands. Although the nucleation of parasitic islands could not be completely inhibited, the yield of NWs could be increased to about 0.5 by proper choice of growth and annealing temperatures.
- We assess the role of substrate preparation, showing that a range of InAs NW densities can be obtained by modifying in situ growth and ex situ sputtering parameters.