



Quantum transport in dual-channel InAs/InP/GaAsSb core-shell nanoscale devices

and Graphene/unltrathin-Si₃N₄ heterostructure device

Sedighe Salimian





- > Where we are..
- > Experimental results
- Device Structure
- InAs/InP/GaSb core-dual shell NWs; application
- > InAs/GaSb heterostructure; application
- > Broken-gap; Negative differential resistance
- III-V heterostructures NW with broken gap

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III-V heterostructures NW ; application







Appl. Phys. Lett. 101, 103501 (2012)





Tunable Esaki Effect in Catalyst-Free InAs/GaSb Core—Shell Nanowires

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Coulumb drag systems







Coulumb drag systems













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Growth and Strain Relaxation Mechanisms of InAs/InP/GaAsSb Core-Dual-Shell Nanowires

Omer Arif, Valentina Zannier,* Ang Li, Francesca Rossi, Daniele Ercolani, Fabio Beltram, and Lucia Sorba





Electrical transport



Au

➤Shell-Shell configuration

Finding the practical thickness of InP barrier

≻Multi-terminal core-shell devices

Studying the impact of InP barrier







Shell-Shell configuration









Selective area etching CDS Nanowire



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- Selective area etching from GaAsSb and InP
- 165 mm Etchant calibration **GaAsSb** and **InP** shells ≻NW geometry Interface with substrate



Selective area etching CDS Nanowire







Multiterminal Core-Shell device







ISSN 1998-0124 CN 11-5974/O4 https://doi.org/10.1007/s12274-020-2745-5

Electrical probing of carrier separation in InAs/InP/GaAsSb core-dualshell nanowires

Sedighe Salimian¹ ([]), Omer Arif¹, Valentina Zannier¹, Daniele Ercolani¹, Francesca Rossi², Zahra Sadre Momtaz¹, Fabio Beltram¹, Sefano Roddaro^{1,3}, Francesco Rossella¹ ([]), and Lucia Sorba¹





Where we are..



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Graphene/unltrathin-Si₃N₄ heterostructure device





Ζ.

- Why β -Si₃N₄
- Device structure
- STM on graphene/ β –Si₃N₄ device
- Magneto-transport measurements



Why high-k Dielectric ?

✓ Preserving the intrinsic mobility

✓ Minimizing operation voltage



F. Pizzocchero etal. Nature Com. (2016)





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PISA

B. Chamlagain etal. 2D Mater. (2017)





Si₃N₄ Potential



Z3

Lattice mismatch (G/Si₃N₄)= 3.66 %
$$\mathcal{E} = 6.6$$
 Eg= 5.3 eV



Yang etal. AIP Advances (2011)

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Lattice mismatch (G/hBN)= 1.8 %

Ttrong etal. Nature Nanotech. (2016)



The β -Si₃N₄(0001)/Si(111) substrate; STM, LEED





Less than 1nm thick large area crystalline β -Si₃N₄

Graphene on β -Si₃N₄(0001)/Si(111)



Graphene on β–Si₃N₄(0001)/Si(111); Raman Spectroscopy









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Z



Graphene on β -Si₃N₄(0001)/Si(111): STM, STS



Z



Magnetotransport measurement

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Device structure



Ζ;







Electrical transport at 4.2 K



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The Origin of second Dirac Point...



5.





Magnetotransport measurement

2.0x10¹³

1.5x10¹³

1.0x10¹³

5.0x10¹²

0.0

600

400

200

0

-15

-10

-5

Mobility μ (cm²/(Vs))

Carrier Concentration n (cm⁻²)

 $R(B) - \langle R \rangle_{B}$



10

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Back Gate Voltage V_{BG} (V) National Enterprise for nanoScience and nanoTechnology

0

15

20

54





Field Effect and Hall Effect



3:





Temperature dependence leakage current







In a Nutshell



- *Large* area grown *Crystaline* β -Si₃N₄(0001)
- Observation of *charge carrier modulation*
- Very low leakage current at 4.2 K in this ultrathin high-k Dielectric



Temperature dependence leakage current

FULL PAPER



Morphology and Magneto-Transport in Exfoliated Graphene on Ultrathin Crystalline β -Si₃N₄(0001)/Si(111)

Sedighe Salimian, Shaohua Xiang, Stefano Colonna, Fabio Ronci, Marco Fosca, Francesco Rossella, Fabio Beltram, Roberto Flammini,* and Stefan Heun*

This work reports the first experimental study of graphene transferred on β -Si₃N₄(0001)/Si(111). A comprehensive quantitative understanding of the physics of ultrathin Si₃N₄ as a gate dielectric for graphene-based devices is provided. The Si₃N₄ film is grown on Si(111) under ultra-high vacuum (UHV) conditions and investigated by scanning tunneling microscopy (STM). Subsequently, a graphene flake is deposited on top of it by a polymer-based transfer technique, and a Hall bar device is fabricated from the graphene flake. STM is employed again to study the graphene flake under UHV conditions after device fabrication and shows that the surface quality is preserved. Electrical transport measurements, carried out at low temperature in magnetic field, reveal back gate modulation of carrier density in the graphene channel and show the occurrence of weak localization. Under these experimental conditions, no leakage current between back gate and graphene channel is detected.



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