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INTERFACIAL ENGINEERING IN BLUE-GREEN LASERS

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ABSTRACT

Although blue-green lasers based on wide-gap II-VI semiconductors have been demonstrated, the development of a viable laser technology hinges on our ability to characterize and improve the properties of a number of crucial heterostructures. Here we report studies of the structural and electronic properties of II-VI/III-V heterostructures as well as metal/II-VI contacts. The results allowed us to propose a number of novel microscopic engineering methods. These include control of the local interface composition to tune the band discontinuities and minimize the defect density and exploitation of graded interface layers and local dipoles to reduce the specific contact resistance.

INTRODUCTION

Since the first demonstration of a pulsed blue-green laser operating at liquid nitrogen temperature in 1991 [1,2], substantial progress has been made toward the implementation of a viable blue-green solid state laser technology. Such a technology is in high demand for applications ranging from optical information storage to xerography and full-colour display, printers and projection systems. Although some recent successes have been obtaining utilizing group III nitrides, [3] most devices demonstrated to date are comprised of wide-gap II-VI epitaxial layers grown by molecular beam epitaxy (MBE) on III-V buffers, and include highly strained $Zn_{1-x}Cd_xSe$ ternary quantum wells embedded in unstrained waveguiding and cladding layers.[4-9] In some structures, lasing operation in the cw mode at room temperature has been demonstrated for a hundred hours.[6]

The short lifetime for cw operation at room temperature, and low efficiency of existing emitters are interface-related.[10,11] Problems include stacking fault defects [12,13] and strain [14] at the II-VI/III-V interface involved in laser degradation, the poor hole injection across the interface between the GaAs substrate and the ZnSe-based epitaxial layers, and the high contact resistance of metal junctions to ZnSe or related materials.[15-17]

We report here on different methods to reducing or eliminating such limitations by exploiting new interfacial engineering principles.[18] For II-VI/III-V heterojunctions, we varied the local interface composition to optimize the band alignment.[19-21] Theoretical developments have been instrumental in clarifying the role of heterovalent heterojunctions with polar orientation as the most likely candidates for tuneable interfacial systems.[22-26]

In, addition, we found that the local interface composition has an important effect on the nucleation of native stacking faults at the interface.[27]

For metal contacts to II-VI material, we examine two different methods to vary the Schottky barrier and reduce the contact resistance. The first method exploits graded composition ternary layers at the interface,[28,29] the second employs instead local interface dipoles fabricated by varying the local interface composition to change the band alignment across the interface.[29]

EXPERIMENTAL DETAILS

All heterostructures were fabricated by solid source MBE in a dedicated system with interconnected chambers for II-VI and III-V semiconductor growth, following the methods described elsewhere.[19,20,33] The substrates were GaAs(001) wafers, on which 500nm-thick GaAs(001)2x4 buffer layers were grown at 580°C. ZnSe overlayers were deposited at 290°C on the GaAs buffers. $Zn_{1-x}Cd_xSe$ epilayers were typically grown instead at 250°C. We used different values of the Zn/Se beam pressure ratio (BPR) during II-VI growth, as determined from ion gauges positioned at the sample location. The local composition was determined in-situ by means of monochromatic x-ray photoemission spectroscopy (XPS). The spectrometer uses Al K_α radiation and a crystal monochromator to achieve a typical resolution of 0.7eV, for a photoelectron escape depth of 1.5nm. The band alignment across each interface was determined in-situ by XPS and confirmed ex-situ through transport methods on selected structures or devices. Information on the structural properties of the different interfaces was obtained in-situ using reflection high energy electron diffraction (RHEED) at 10 KeV, and ex-situ by means of transmission electron microscopy (TEM) [27] and atomic force microscopy (AFM).[14.34]

RESULTS AND DISCUSSION

A. II-VI/III-V interfaces

As prototypic interfaces we examined ZnSe/GaAs(001) heterostructures, which are pseudomorphic for ZnSe epilayer thicknesses below 150 nm, and $Zn_{1-x}Cd_xSe/In_yGa_{1-y}As$ (001) heterojunctions, which are ideally lattice-matched for appropriate values of x and y. In both systems we found that the BPR employed during II-VI growth has a major effect on the local interface composition. We plot in Fig. 1 the local Zn/Se ratio R, as a function of ZnSe overlayer thickness in ZnSe/GaAs(001) heterojunctions.[10,11,19] Different symbols show the effect of different BPR's in the 0.1 to 10 range. R was determined from the XPS ratio of the integrated emission of the Zn 3d and Se 3d doublets, normalized to the value observed in all ZnSe bulk standards, irrespective of the BPR. The values of R in the first few monolayers exhibit large variations from the nominal 1:1 stoichiometry. Large Zn overpressures (high BPR's) during growth correspond to Zn-rich interface compositions, while large Se overpressures (low BPR's) correspond to Se-rich interface compositions. The amount of excess Zn (or Se) at the interface that can account for the observed behaviour needs not to be large. It is possible to show that the observed deviations of R from unity as a function of ZnSe overlayer thickness would be consistent with excess Zn (or Se) elemental concentrations at the monolayer level, below an essentially stoichiometric II-VI overlayer. Results for the Ga 3d and As 3d emission do not show conclusively any deviation from stoichiometry at the result of the presence of excess Zn (or Se). However, the Ga and As signals from the interface appear always superimposed to a dominant bulk contribution, unlike the Zn and Se signals. The sensitivity to variations in the Ga/As ratio is therefore comparatively low.[10,11,19]

In Fig. 2 we show valence band offsets determined using the measured energy separation of overlayer and substrate core levels across the interface at a coverage of 2-3 nm, and the position of the same core levels relative to the top of the valence band maximum in

bulk standards, for a number of heterojunctions grown on GaAs(001) substrates. The offsets are plotted versus the value of R observed in the early stages of interface formation, i.e. at an arbitrary ZnSe coverage of 0.3nm. Different symbols denote data obtained using substrates with different type of doping. Unless noted otherwise, all GaAs(001) surface reconstructions were 2x4. The experimental valence band offsets in Fig. 2 show a remarkably good correlation with the value of R near the interface. Zn-rich interface compositions correspond to valence band offsets as large as ~1.2eV, while Se-rich interface compositions correspond to offsets as low as ~0.6eV.[10,11,19]

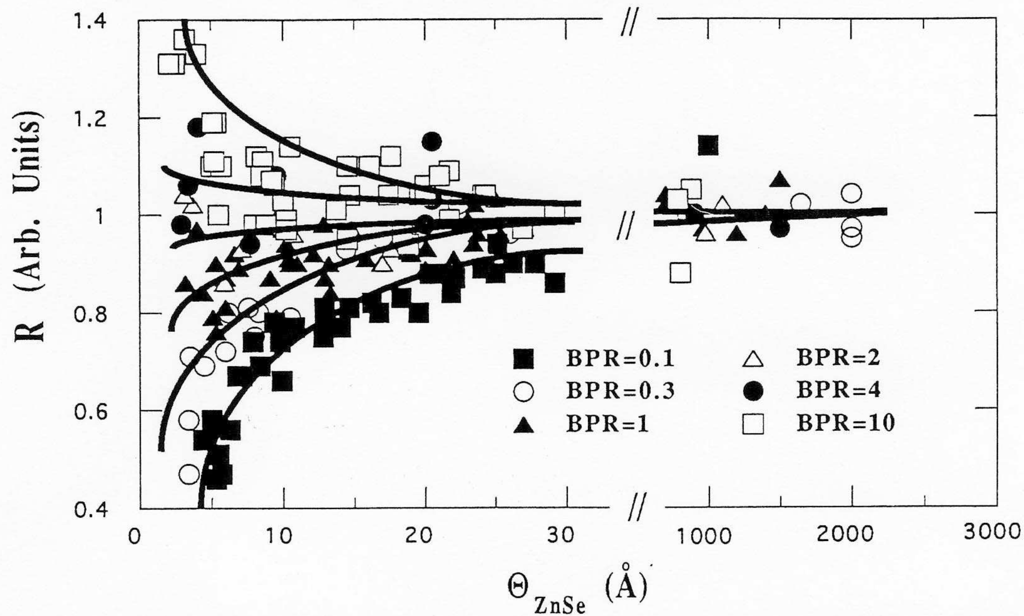

Fig. 1. Experimental Zn/Se photoemission intensity ratio R in ZnSe-GaAs(001) heterojunctions grown by MBE with different Zn/Se beam pressure ratios (BPR's), as a function of ZnSe thickness.

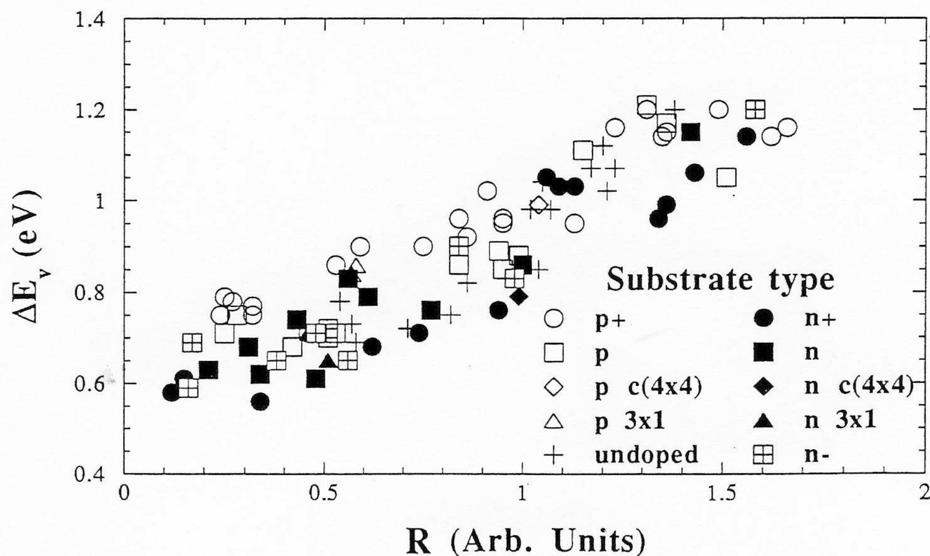

Fig. 2. Experimental valence band offset for ZnSe-GaAs(001) heterojunctions as determined by XPS, as a function of the Zn/Se ratio R at the interface.

First principle calculations allow us to establish possible connections between the measured band alignment and the local interface configuration.[19,26,35] Since ideally abrupt heterovalent interface with (001) orientation would be charged, and therefore thermodynamically unstable [22-26], atomic intermixing has to be called upon to form neutral configurations. Some of the simplest possible configurations would involve atomic mixing on one or two atomic planes at the interface. A 50-50 mixing of anions (Se-As) or cations (Zn-Ga) on a single plane at the interface would yield neutral interfaces with the same formation enthalpy [35] and extreme values (0.62 and 1.59 eV, respectively) for the valence band offsets, since the ionic dipoles at the interface would be of equal magnitude and opposite orientation.[19,26] Other particular interface configurations would make the ionic dipole vanish, as it would be the case for abrupt non-polar {110} interfaces. For example, two adjacent mixed planes at the interface with Se-As 25-75 and Zn-Ga 75-25 composition would cancel the ionic dipole, yielding a calculated valence band offset of 1.17 eV, i.e., identical to that predicted for the non polar {110} interface orientations.[19,22-26,35]

The range of predicted variability of the offset (0.62-1.59 eV) is compellingly similar to that observed experimentally in Fig. 2, but we caution the reader that the calculations examined only a few of the infinite possible interface reconstruction that would lead to neutral interfaces. Although one would be tempted to associate the low valence band offset observed for Se-rich growth conditions (~0.6eV) with a Se-As intermixed interface (predicted offset 0.62eV), and the high offset observed for Zn-rich conditions (~1.2eV) with cation-mixed configurations (predicted offset 1.59 eV), at this stage we have no information on the relation between the R parameter in Fig. 2, and the corresponding Ga/As ratio, so that we cannot prove or disprove that the configurations examined by theory are achieved in practice.[11,19]

The dependence of the band alignment on the interface composition has been quantitatively confirmed by recent internal photoemission [36] and low-temperature tunnelling measurements.[21] In both experiments, ZnSe/GaAs(001) interfaces buried well below the sampling depth of XPS were examined, and transport of photoinjected carriers across the conduction band discontinuity was probed by optical [36] or electrical [21] methods. The results were quantitatively consistent with those obtained in the thin-layer samples by XPS in the earlier experiments.[19,20] The remarkable agreement suggests that the metastable interface configurations responsible for band offset tuning in the thin-overlayer samples [19,20] are sufficiently stable to sustain the following stages of device fabrication and processing so that they can be exploited in fully functional devices, such as the p-n heterodiodes of Ref. 21.

Low valence band offsets in II-VI/III-V heterojunctions are desirable to enhance hole injection in electroluminescent devices. However, the fabrication of Se-rich interface requires one to use relatively low BPR's (0.1-0.2) during ZnSe growth while minimization of unintentional doping and dislocation density in ZnSe requires BPR's relatively close to unity.[37-38] Also, heterostructures fabricated in Se-rich conditions appear less stable than those obtained in stoichiometric or Zn-rich conditions, since annealing at relatively low temperatures (300-350°C) gives rise to a strong enhancement in the deep level emission [39] from Zn vacancies, or complex defect centers involving Zn vacancies and substitutional Ga atoms on Zn sites. [29,30]

Achieving engineered valence band offsets without degrading the II-VI overlayer quality is, however, possible by exploiting the local character of the interface changes that lead to band offset tuning. In fact, changes in band alignment compellingly similar to those in Fig. 2 were also obtained when the nonstoichiometric growth conditions (Se- or Zn-rich) were employed only for a thin (2 nm-thick) composition control interface layer (CIL), while the bulk of the II-VI epilayer was grown with BPR=1.[20,21] Also, recent high resolution synchrotron radiation photoemission studies have shown that exposing the III-V substrate surface to a Se or Zn flux at a temperature low enough for ordered monolayers of Se or Zn to form [40,41] prior to II-VI growth results in similar offset variations.[40]

The local interface composition in II-VI/III-V heterojunctions has also a strong effect on the structural properties of the overall heterostructure. Strain relaxation [42] and the density of native stacking faults [27] are both found to be affected by the interface termination. The second issue is especially relevant because stacking faults at the II-VI/III-V

interface may strongly influence device degradation by propagating through the structure during growth and generating dislocation sources within the strained active layers.[43-47]

The existence of relatively high densities of native stacking faults at ZnSe/GaAs and related interfaces has been known for quite some time. Both intrinsic and extrinsic stacking faults have been reported,[44] bounded by Frank [43-44,46] or Shockley [44,45] partial dislocations. Attempts at reducing the native stacking fault concentration have produced intriguing results. MBE studies have reported a high density (10^8cm^{-2}) of stacking faults if the III-V surface was exposed initially to a flux of elemental Se, while exposure to a Zn flux prior to II-VI growth lead to much lower stacking fault densities.[43,44] Based on RHEED results, this was associated with the nucleation of three-dimensional (3D) islands in the early stages of II-VI growth on Se-predosed surfaces as opposed to two-dimensional (2D) growth on Zn-predosed surface.[43,44,46] However, a recent study of pseudomorphic ZnSe/GaAs(001) heterostructures grown by metalorganic chemical vapor deposition reported an *increase* in the stacking fault density for heterostructures fabricated after exposure to Zn of the As-stabilized substrate, as well as for growth on surfaces on which excess As was present.[47]

We examined the effect of the local interface composition on the stacking fault density in both strained, pseudomorphic ZnSe/GaAs(001) heterostructures, as well as in lattice-matched ZnSe-$In_{0.04}Ga_{0.96}As$(001) heterostructures.[27] The Zn/Se BPR employed during the early stages of interface formation was found to have a dramatic effect on the density of stacking faults. For example, TEM studies indicated that pseudomorphic ZnSe/GaAs(001) heterostructures incorporating a Zn-rich CIL (grown with BPR=10) exhibited an areal density of Shockley stacking fault of 7×10^8cm^{-2}, control samples grown with BPR=1 throughout showed a density of Shockley stacking faults 3-4 times lower, while heterostructures incorporating a Se-rich CIL (grown with BPR=0.1), exhibited a Shockley stacking fault density below our TEM detection limit of $1\text{-}2\times10^5$cm^{-2}.

A comparison of the results for ZnSe/GaAs(001) and ZnSe/$In_{0.04}Ga_{0.96}As$(001) heterostructures is shown in Table I. The data clearly indicate that the parameter that most strongly influences the concentration of native stacking faults is the initial BPR, and therefore the composition of the interface region, as opposed to overlayer thickness or strain.

Sample	ZnSe (nm)	CIL (BPR)	Shockley (cm^{-2})	Frank (cm^{-2})	Threading (cm^{-2})
ZnSe/GaAs, #499	100	10	5.6×10^8	2.3×10^7	$\sim6\times10^7$
ZnSe/GaAs, #323	100	10	7.0×10^8	3.0×10^6	$<2\times10^5$
ZnSe/InGaAs, #510	100	10	7.0×10^8	1.8×10^6	$<2\times10^5$
ZnSe/InGaAs, #501	300	10	1.5×10^8	7.0×10^6	$<2\times10^5$
ZnSe/GaAs, #326	100	1	2.0×10^8	5.0×10^7	$<2\times10^5$
ZnSe/GaAs, #488	100	1	2.6×10^6	7.5×10^5	$\sim2\times10^6$
ZnSe/InGaAs, #514	300	1	1.0×10^7	2.6×10^6	$\sim3\times10^6$
ZnSe/GaAs, #330	100	0.1	1×10^5	2.0×10^6	$<2\times10^5$
ZnSe/GaAs, #504	100	0.1	$<5\times10^4$	2.4×10^6	$<5\times10^4$
ZnSe/InGaAs, #505	100	0.1	$<2\times10^5$	$<2\times10^5$	$<2\times10^5$
ZnSe/InGaAs, #508	300	0.1	$<2\times10^5$	2.2×10^6	$<2\times10^5$

Table I. Representative results for the areal density of Shockley stacking fault pairs (column 4), Frank stacking faults (column 5), and threading dislocations (column 6), for different ZnSe/GaAs(001) and ZnSe/$In_{0.04}Ga_{0.96}As$(001) heterostructures (column 1) with ZnSe overlayer thickness of 100 or 300nm (column 2), and incorporating a 2nm-thick CIL grown with a Zn/Se beam pressure ratio (BPR) of 10 or 0.1, or fabricated with BPR=1 throughout (column 3). The experimental sensitivity was 2×10^5cm^{-2} unless noted otherwise.

The majority of the stacking faults are Shockley stacking fault pairs, but their number decreases by *at least* three to four orders of magnitude in going from Zn-rich to Se-rich interfaces. The minimum stacking fault densities in Table I compare favorably with the best results reported to date.[43-47]

The density of Frank stacking faults is also affected by the interface composition, although to a lesser extent. A decrease in the density of Franck stacking faults by a factor of 5 to 10 is typically observed when comparing heterostructures with Zn- and Se-rich interfaces. The implication is that the microscopic mechanism behind the formation of Shockley and Frank stacking faults at II-VI/III-V interface might be qualitatively different, although both are influenced by the Zn/Se atomic flux ratio employed in the early stage of interface formation.[27]

We emphasize that the mechanism through which the initial BPR affects the stacking fault nucleation rate is likely to be related to the effect of the different resulting interface configuration on the stacking fault nucleation energy, rather than that proposed by other authors [43,44,46] to explain the effect of Se- or Zn-predosing. First, Se-rich CILs were found here to correspond to lower stacking fault densities, while *higher* stacking fault densities were observed as a result of ZnSe growth on Se-predosed GaAs surfaces.[43,44,46] Second, previous studies [43,44,46] report that ZnSe growth on Se-predosed surfaces gives rise to a characteristic RHEED pattern indicative of 3D growth, while we observed qualitatively similar 2D growth during fabrication of Se-rich and Zn-rich CILs.[27]

B. Metal/semiconductor junctions

For most technologically relevant metals on Si and GaAs surfaces, the pinning position of the Fermi level upon metal deposition is near the midgap energy, and contacts with sufficiently low contact resistance can be fabricated by doping heavily the semiconductor region closest to the metallurgical interface, and achieve tunnelling.[48] Unfortunately, the wide gap of ZnSe and the present limitation in doping technology for ZnSe-related materials combine to give unacceptably high contact resistance and therefore dissipation. A Schottky barrier some 3-10 times *lower* than those encountered on Si or GaAs would be presently required to achieve comparable specific contact resistance in view of the present limitation of ZnSe doping technologies.[10] Since the specific contact resistance varies exponentially with the ratio of the barrier height to the square root of the doping concentration,[48] any lowering the Schottky barrier value would have a strong effect on this figure of merit.[10]

One avenue that we have recently explored is the introduction of graded composition ternary layers at the interface. In particular, we used n^+-$Zn_{1-x}Cd_xSe$ interface layers to optimize Al/n-ZnSe junctions. Our interest in this was stimulated by three main considerations. First, the ternary alloy $Zn_{1-x}Cd_xSe$ can be grown epitaxially on ZnSe by MBE and exhibits a bandgap which decreases monotonically with increasing Cd concentration x. Second, recent studies indicate that the conduction band discontinuity accounts for most (70-80%) of the $Zn_{1-x}Cd_xSe$/ZnSe bandgap difference.[50] Third, among the technologically relevant metals, aluminum is known to exhibit one of the lowest Schottky barriers to n-type ZnSe.[49]

From synchrotron radiation photoemission measurements of the Schottky barriers in Al/$Zn_{1-x}Cd_xSe$(001)1x1 junctions we obtained n-type barriers $\Phi_{bn0}=0.78\pm0.04$, 0.58 ± 0.10, and 0.45 ± 0.04eV, for samples with x=0, 0.2, and 0.3, respectively.[28,29]. In view of the drastic reduction (42%) of Φ_{bn0} in going from Al/ZnSe to Al/$Zn_{0.7}Cd_{0.3}Se$ junctions, comparable doping in the two junctions should give rise to substantially lower contact resistance in the second type of junction, provided that the results for interfaces prepared in ultra-high-vacuum conditions apply to technological contacts. We therefore performed current-voltage (I-V) measurements on a number of Al/$Zn_{1-x}Cd_xSe$ contacts fabricated with standard photolithographic techniques on air-exposed substrates. A 300nm thick Al layer was evaporated on $Zn_{1-x}Cd_xSe$ substrates with different values of x (ranging

from 0 to 0.3) and n (ranging from $4x10^{18}$ cm^{-3} to $2x10^{19}$ cm^{-3}). Contacts were patterned with standard photolithographic and lift-off techniques.

The specific contact resistance was derived from the I-V data using the transmission line approach.[28] The experimental results are summarized in Fig. 3, together with the theoretical specific resistance that would be expected or an ideal Al/$Zn_{1-x}Cd_xSe$ metal-semiconductor junction taking into account both thermionic and tunnelling current based on the photoemission-determined Schottky barrier values. Taking into account the experimental uncertainty, the agreement between the experimental data and the predictions in Fig. 3 is remarkable, and clearly demonstrates that the observed decrease in the contact resistance with increasing x is the result of the type of band alignment envisioned.

The lowest contact resistance in Fig. 3 ($1.5\pm0.5x10^{-5}$ $\Omega\cdot cm^2$) is, to our knowledge, the lowest ever reported for a n-type ZnSe-based, wide gap semiconductor. The implication is that fabrication of a $Zn_{1-x}Cd_xSe$ interface layer in a Al/n-ZnSe junction will change the contact resistance in view of the resulting grading of the conduction band offset, and that Fig. 3 can be used to predict the resulting contact resistance. This is exemplified in the inset of Fig. 3, where we show the forward I-V characteristics (open circles) for an Al/n-$Zn_{1-x}Cd_xSe$/n-ZnSe/p-GaAs heterostructure incorporating a 500nm-thick ternary graded layer. The Cd concentration x was varied linearly from x=0.3 at the surface to x=0 in the bulk. $Zn_{1-x}Cd_xSe$ doping was n~$7x10^{18}$ cm^{-3}, while for ZnSe it was n~$1x10^{18}$ cm^{-3} and $1x10^{16}$ cm^{-3}, in the bulk and in the p-n junction region, respectively. GaAs doping was $1x10^{18}$ cm^{-3} and $1x10^{16}$ cm^{-3}, in the bulk and in the p-n junction region, respectively. The

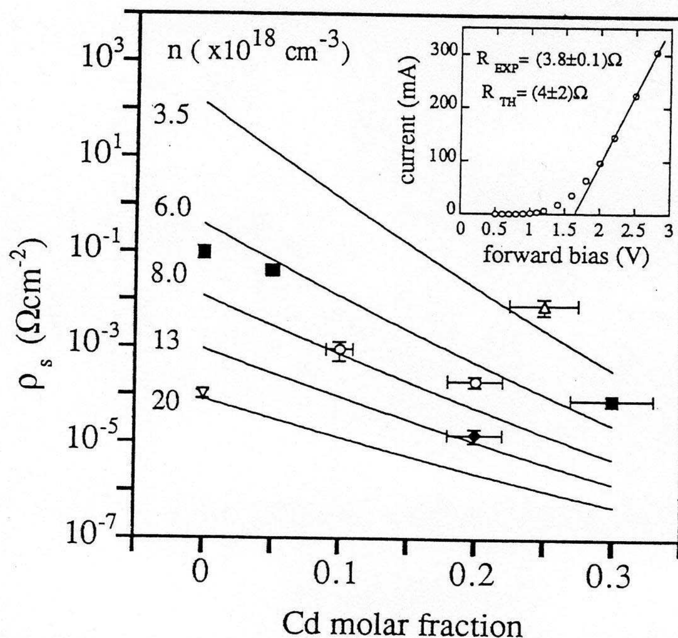

Fig. 3 Specific contact resistance for Al-$Zn_{1-x}Cd_xSe$ junctions as a function of Cd content and doping levels. Experimental results (symbols) and theoretical results (solid line) are compared. Different symbols are related to different doping levels in the following way: (Δ) $4.0\pm0.5x10^{18}$ cm^{-3}; (■) $6.5\pm0.7x10^{18}$ cm^{-3}; (O) $9\pm1x10^{18}$ cm^{-3}; (♦) $1.4\pm0.2x10^{19}$ cm^{-3}; (∇) $2.0\pm0.2x10^{19}$ cm^{-3}. The doping level marked to the left of each line denotes the value used in the calculations. Inset: experimental current-voltage (I-V) curve for a n-ZnSe/p-GaAs diode incorporating a graded Al/$Zn_{1-x}Cd_xSe$ contact to the ZnSe layer. The slope of the forward I-V characteristic in the linear range is consistent with an upper limit of 3.8Ω for the contact resistance, to be compared with a value of 4±2Ω predicted from the model.

contact was a 50nm diameter Al dot. The forward current in the overall heterostructure shows a turn-on voltage of the order of 1 V due to the ZnSe-GaAs p-n junction, and an approximately linear I-V relation in the 2-3 V range. The slope in the linear range is consistent with an upper limit for the experimental contact resistance of 3.8±0.1Ω, to be compared with a value of 4±2Ω predicted from the model.

A second possible method to change the Schottky barriers would use appropriate changes of the local interface termination to fabricate an additional local interface dipole.[10] In principle, the same type of electrostatic arguments about interface dipoles presented in the previous section for semiconductor heterojunctions, and their effect on the band alignment across an interface can also be made for metal/semiconductor junctions. There is already evidence in hand that the initial surface termination can affect the Schottky barrier in metal/ZnSe junctions. For example, the value of the p-type Schottky barrier that we measured following Al deposition on the ZnSe(001)1x1 surface, which is known to be Se-terminated, was some 0.20 eV lower than that observed following Al deposition on the Zn-stabilized c(2x2) reconstruction of ZnSe(001).[49,51] We emphasize that the difference reflects a true change in the pinning position of the Fermi level, rather than photovoltage effects, or a different method to determine the core level binding position relative to valence band maximum E_V.[29]

In similar experiments on Au/ZnSe(001) interfaces, other authors have also observed a 0.25eV lower p-type Schottky barrier when Se-rich surfaces - as opposed to the Zn-rich c(2x2) surface - were employed.[52] These exciting results remains unexploited to date in device-grade structures in view of the difficulty of controlling the initial semiconductor interface termination in the metallization systems used in industry.

Recently, methods to reproducibly change the Schottky barrier height at metal/semiconductor interfaces by means of thin heterovalent interlayers have been demonstrated for III-V semiconductors.[30-32] The Schottky barrier was tuned by fabricating a thin (1 to 4 monolayer thick) Si layer by MBE in the interface region of Al/n-GaAs(001) diodes. A relative large excess flux of anions (As) or cations (Al) was used during Si deposition at 300°C onto the GaAs(001)2x4 substrates. It was found by both in-situ photoemission methods and ex-situ I-V measurements that the presence of a Si interlayer grown under As flux yielded a substantial decrease of the n-type Schottky barrier, and therefore a substantial increase in the p-type barrier at the interface. The presence of a Si interlayer grown under an excess cation flux had the opposite effect. The minimum value of the n- and p-type Schottky barriers obtained with such methods were 0.20-0.25eV, with a variation of ±0.5eV relative to the control contacts with no heterovalent interlayers, provided that high enough excess cation or anion fluxes (comparable to the Si flux) were employed during Si fabrication.

The original explanation of these results in terms of a Si-related microscopic capacitor on an As- versus Ga-terminated semiconductor was recently tested by means of first principle calculations of the local interface dipole in Al/Si/GaAs(001) structures with As- and Ga-terminated semiconductors surface.[53] The theoretical results were found to be in remarkably good agreement with the experimental values [30,31] of the engineered Schottky barriers. As a consequence, we have proposed to extend this method to engineer metal/ZnSe contacts.[10] For example, the use of Ge or Si interface layers grown under excess cation and anion flux should produce a local dipole twice as large at metal/ZnSe interfaces as compared to those observed at metal/III-V junction, in view of the larger valence difference between the two semiconductors.[10]

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